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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,406	09/26/2003	Ying-Lang Chuang	3304.2.89	9139

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EXAMINER	
TON, MY TRANG	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,406	CHUANG, YING-LANG	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-21 and 32* is/are rejected.

7)☒ Claim(s) *22-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MY-TRANG NU TON
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. In response to Applicant's amendment filed on January 10, 2005, the rejection made in the last Office action on the Chapman's reference is withdrawn.

2. A new Office action has been made as follows:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6, 8-20 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Chuang (U.S Patent No. 6,690,219).

Chuang discloses in Fig. 4 a digital wave generating apparatus including:

Regarding claim 1:

providing a plurality of source signals (CK0-CK19...), every adjacent two of which have a phase difference of a certain clock unit (delay phase lock loop 402 provides CK0-CK19);

duplicating the source signals to obtain a first and a second signal groups (OUT2 is duplicate of CK0-CK19, OUT1 is duplicate of output signal from 402);

generating a first and a second output signals at a first and a second time points based on the first and the second signal groups, respectively (F2, F1 generates Q-F1, Q-F1 based on signals output from 402 (first group) OUT2, OUT1 (second group)); and

processing the first and the second output signals (Q-F1, Q-F2) by a logic operation (409) to obtain the delay signal (W).

Regarding claim 2: the plurality of source signals (CK0-CK19) are generated from a high-frequency signal by a phase-locked loop device (402).

Regarding claim 3: the plurality of source signals (CK0-CK19) are a series of increasingly lagging signals (see Fig. 5, timing diagram for CK0-CK19).

Regarding claim 4: the plurality of source signals (CK0-CK19) are a series of increasingly leading signals (see Fig. 5, timing diagram for CK0-CK19)

Regarding claim 5: the logic operation is an XOR operation (409).

Regarding claim 6: the steps of generating the first and second output signals (Q-F1, Q-F2) comprises sub-steps of:

selecting (M2) a signal from the first signal group (signals output from 402) at the first time point as the first output signal; and

selecting (M1) a signal from the second signal group at the second time point as the second output signal.

Regarding claim 8: the first and the second time points are predetermined, and located by counting operations (F1, F2) in response to a first and a second clock signals (OUT2, OUT1), respectively.

Regarding claims 9-12: because the claimed structure is fully met by Chuang, the functions recited therein will necessarily be inherent in Chuang, as held by the court in In re Best, 195 USPQ 430.

Regarding claim 13: first and the second signal groups are divided into a first and a second plurality of signal sub-groups (fist group: signals from the output of 402, second group: OUT2, OUT1 are divided into a first and second plurality of signal sub-group), and the first and the second output signals (Q-F1, Q-F2) are generated from one of the first plurality of signal sub-groups and one of the second plurality of signal sub-groups, respectively.

Regarding claim 14: all source signals in the selected one of the first plurality of signal sub-groups (CK0-CK19 ...) are at the same first level at the first time point, and all source signals in the selected one of the second plurality of signal sub-groups (OUT2, OUT1) are at the same level at the second time point.

Regarding claim 15: because the claimed structure is fully met by Chuang, the function recited therein will necessarily be inherent in Chuang, as held by the court in In re Best, 195 USPQ 430.

Claim 16 is similarly rejected as above:

a source signal generator (402) generating and outputting N counts of source signals (CK0-CK19) in response to a high frequency signal, every adjacent two of the N counts of source signals having a phase difference of a certain clock unit;

a source-signal selector (M2, M1, 404, 405, 406, 408, F1, F2) coupled to the source signal generator (402) , and selecting a first and a second ones of the N counts of source signals (CK0-CK19) to be outputted at a first and a second time points in response to a first and a second clock signals (OUT 2, OUT1) as a first and a second outputs signals (Q-F2, Q-F1), respectively, and

a logic operator (409) coupled to the source signal selector (M2, M1, 404, 405, 406, 408, F1, F2) and logically operating the first and the second output signals (Q-F2, Q-F1) to obtain the delay signal (W).

Regarding claim 17: the source signal generator is a phase locked loop device (402).

Regarding claim 18: element 402 reads on a selection-signal generating circuit; element M2 reads on a first multiplexing circuit and element M1 reads on a second multiplexing circuit.

Regarding claim 19: elements M1-M2 read on the first and second multiplexing circuit performing the function recited therein.

Regarding claim 20: element 404 reads on a first signal synthesizing circuit; and element 405 reads on a second signal synthesizing circuit.

The method recited in claim 32 is similarly rejected as claims 1 and 16:

providing a plurality of source signals (delay phase locked loop 402 provides a plurality of source signals CK0-CK19), every adjacent two of which have a phase difference of a certain clock unit;

generating (M2, M1, 404, 405, 406, 408, F1, F2) a first and a second output signals (Q-F2, Q-F1) at a first and a second time points based on the plurality of source signals (CK0-CK19), wherein the first and second time points are predetermined and located by counting operations (F2, F1) in response to a first and a second clock signals (OUT2, OUT1), respectively; and

processing the first and the second output signals (Q-F2, Q-F1) by a logic operation (409) to obtain the delay signal (W).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chuang as applied to claims 16-20 above.

As stated above, every element of the claimed invention recited in above claims can be seen in the circuit of Chuang. However, this reference does not specifically show the "first and said second synthesizing circuits includes an OR gate" (claim 21).

Nevertheless, the OR gate are well-known logic devices and patentable equivalent to the AND gate (404, 405 of Chuang) since no unobvious results are seen produce from there use. Therefore, it would have been obvious at the time of the invention was made for one skilled in the art to utilize these particular types of logic gate (substitute OR gate for 404, 405) since it is notoriously well known in the art.

Allowable Subject Matter

Claims 22-31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims

namely: the details of the first synthesizing circuit in combination with the details of the second synthesizing circuit as recited in claim 22; the details of the selection signal generating circuit as recited in claim 25; the combination of "the storage unit" and "the logic operation unit" as recited in claim 28.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

My-Trang N. Ton
Primary Examiner
Art Unit 2816

March 30, 2005